

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A method of exporting emulation
2 information from a data processor integrated circuit, comprising:
3 collecting internal emulation information from a data
4 processor ~~at a data processor clock rate;~~
5 arranging the collected emulation information into a plurality
6 of first information blocks organized in a sequence, each of said
7 first information blocks having a first fixed size, wherein a first
8 number of consecutive ones of said first information blocks defines
9 a sequence of consecutive bits of said emulation information, and
10 wherein each of said first number of consecutive first information
11 blocks defines part of said sequence of consecutive bits;
12 receiving the plurality of first information blocks and
13 arranging the emulation information contained therein into a
14 plurality of second information blocks organized in a sequence,
15 each of said second information blocks having a second fixed size
16 which differs from the first fixed size of the first information
17 blocks, wherein a second number of consecutive ones of said second
18 information blocks defines said sequence of consecutive bits,
19 wherein each of said second number of consecutive second
20 information blocks defines part of said sequence of consecutive
21 bits, and wherein said second number differs from said first
22 number; and
23 outputting [a] said sequence of [the] second information
24 blocks from the data processor integrated circuit ~~via a plurality~~
25 ~~of terminals at a transmission clock rate, said first fixed size,~~
26 ~~said data processor clock rate, said second fixed size and said~~
27 ~~transmission clock rate related whereby a bit rate of first~~

28 ~~information blocks equals a bit rate of said second information~~
29 ~~blocks to a host external to the data processor integrated circuit.~~

1 2. (Previously Presented) The method of Claim 1, wherein the
2 second fixed size is smaller in size than the first fixed size.

1 3. (Original) The method of Claim 1, including receiving the
2 sequence of second information blocks externally of the data
3 processor, and re-arranging the emulation information contained in
4 the second information blocks into a plurality of the first
5 information blocks.

1 4. (Original) The method of Claim 1, wherein each of the
2 first and second information blocks is a packet of emulation
3 information.

5 to 15. (Cancelled)

1 16. (Currently Amended) An integrated circuit, comprising:
2 a data processor for performing data processing operations;
3 a collector coupled to said data processor for collecting
4 emulation information from said data processor ~~at a data processor~~
5 ~~clock rate~~ and arranging said emulation information into a
6 plurality of first information blocks organized in a sequence, each
7 of said first information blocks having a first fixed size, wherein
8 a first number of consecutive ones of said first information blocks
9 defines a sequence of consecutive bits of said emulation
10 information, and wherein each of said first number of consecutive
11 first information blocks defines part of said sequence of
12 consecutive bits;

13 an exporter coupled to said collector for receiving therefrom
14 said plurality of first information blocks and arranging said

15 emulation information contained therein into a plurality of second
16 information blocks organized in a sequence, each of said second
17 information blocks having a second fixed size which differs from
18 the first fixed size of said first information blocks, wherein a
19 second number of consecutive ones of said second information blocks
20 defines said sequence of consecutive bits, wherein each of said
21 second number of consecutive second information blocks defines part
22 of said sequence of consecutive bits, and wherein said second
23 number differs from said first number;

24 a plurality of terminals for outputting information; and
25 said exporter coupled to said terminals for outputting [a]
26 said sequence of [the] second information blocks via said terminals
27 ~~at a transmission clock rate, said first fixed size, said data~~
28 ~~processor clock rate, said second fixed size and said transmission~~
29 ~~clock rate related whereby a bit rate of first information blocks~~
30 ~~equals a bit rate of said second information blocks.~~

1 17. (Previously Amended) The integrated circuit of Claim 16,
2 wherein said second fixed size is smaller in size than said first
3 fixed size.

Claims 18 to 26. (Canceled)

1 27. (Currently Amended) A data processing system, comprising:
2 an integrated circuit, including a data processor for
3 performing data processing operations;
4 an emulation controller coupled to said integrated circuit for
5 controlling emulation operations of said data processor;
6 said integrated circuit including an apparatus coupled between
7 said data processor and said emulation controller for providing
8 emulation information about said data processing operations, said
9 apparatus including a collector coupled to said data processor for

10 collecting said emulation information from said data processor ~~at a~~
11 ~~data processor clock rate~~ and arranging said emulation information
12 into a plurality of first information blocks organized in a
13 sequence, each of said first information blocks having a first
14 fixed size, wherein a first number of consecutive ones of said
15 first information blocks defines a sequence of consecutive bits of
16 said emulation information, and wherein each of said first number
17 of consecutive first information blocks defines part of said
18 sequence of consecutive bits, and an exporter coupled to said
19 collector for receiving said plurality of first information blocks
20 and arranging said emulation information contained therein into a
21 plurality of second information blocks organized in a sequence,
22 each of said second information blocks having a second fixed size
23 which differs from the first fixed size of said first information
24 blocks, wherein a second number of consecutive ones of said second
25 information blocks defines said sequence of consecutive bits,
26 wherein each of said second number of consecutive second
27 information blocks defines part of said sequence of consecutive
28 bits, and wherein said second number differs from said first
29 number; and

30 said integrated circuit including a plurality of terminals
31 coupled to said emulation controller for outputting information to
32 said emulation controller, said exporter coupled to said terminals
33 for outputting [a] said sequence of [said] second information
34 blocks to said emulation controller via said terminals ~~at a~~
35 ~~transmission clock rate, said first fixed size, said data processor~~
36 ~~clock rate, said second fixed size and said transmission clock rate~~
37 ~~related whereby a bit rate of first information blocks equals a bit~~
38 ~~rate of said second information blocks.~~

1 28. (Original) The system of Claim 27, including a
2 man/machine interface coupled to said emulation controller for
3 permitting a user to communicate with said emulation controller.

1 29. (Original) The system of Claim 28, wherein said
2 man/machine interface includes one of a visual interface and a
3 tactile interface.

1 30. (Previously Presented) The method of Claim 2, wherein:
2 said first fixed size is an integral multiple of said second
3 fixed size; and

4 said step of receiving the plurality of first information
5 blocks and arranging the emulation information contained therein
6 into a plurality of second information blocks includes the steps of

7 (a) storing a current first information block in a
8 current packet register,

9 (b) sequentially selecting groups of the second fixed
10 size bits from the current packet register as a second
11 information block, a first selected group beginning at a first
12 bit of said current packet register, subsequent selected
13 groups beginning at a bit following a last bit of a prior
14 group, until all bits of the current packet register are
15 selected,

16 (c) thereafter storing a next first information block in
17 the current packet register and repeating steps (a), (b) and
18 (c).

1 31. (Previously Presented) The method of Claim 2, wherein:
2 said first fixed size is not an integral multiple of said
3 second fixed size; and

4 said step of receiving the plurality of first information
5 blocks and arranging the emulation information contained therein
6 into a plurality of second information blocks includes the steps of

7 (a) storing a current first information block in a
8 current packet register,

9 (b) sequentially selecting groups of the second fixed
10 size bits from the current packet register as a second
11 information block, a first selected group beginning at a next
12 bit of said current packet register, subsequent selected
13 groups beginning at a bit following a last bit of a prior
14 group, until a number of bits of remaining in the current
15 packet register is less than the second fixed number,

16 (c) storing the current first information block in a last
17 packet register,

18 (d) storing a next first information block in the current
19 packet register,

20 (e) selecting a group of the second fixed size bits from
21 a set of bits remaining in the last packet register and bits
22 starting at a first bit of the current packet register, and

23 (f) thereafter repeating steps (b), (c), (d) and (e).

1 32. (Previously Presented) The integrated circuit of claim
2 17, wherein:

3 said first fixed size is an integral multiple of said second
4 fixed size; and

5 said exporter includes

6 a current packet register, and

7 a combiner connected to said current packet register and
8 said terminals, said combiner operable to

9 (a) store a current first information block in a
10 current packet register,

11 (b) sequentially select groups of the second fixed
12 size bits from the current packet register as a second
13 information block, a first selected group beginning at a
14 first bit of said current packet register, subsequent
15 selected groups beginning at a bit following a last bit
16 of a prior group, until all bits of the current packet
17 register are selected,

18 (c) thereafter store a next first information block
19 in the current packet register and repeat steps (a), (b)
20 and (c).

1 33. (Previously Presented) The integrated circuit of claim
2 17, wherein:

3 said first fixed size is not an integral multiple of said
4 second fixed size; and

5 said exporter includes

6 a current packet register,

7 a last packet register, and

8 a combiner connected to said current packet register and
9 said terminals, said combiner operable to

10 (a) store a current first information block in a
11 current packet register,

12 (b) sequentially select groups of the second fixed
13 size bits from the current packet register as a second
14 information block, a first selected group beginning at a
15 next bit of said current packet register, subsequent
16 selected groups beginning at a bit following a last bit
17 of a prior group, until a number of bits of remaining in
18 the current packet register is less than the second fixed
19 number,

20 (c) store the current first information block in a
21 last packet register,

22 (d) store a next first information block in the
23 current packet register,
24 (e) select a group of the second fixed size bits
25 from a set of bits remaining in the last packet register
26 and bits starting at a first bit of the current packet
27 register, and
28 (f) thereafter repeat steps (b), (c), (d) and (e).

1 34. (Previously Presented) The data processing system of
2 Claim 27, wherein:
3 said second fixed size is smaller in size than said first
4 fixed size.

1 35. (Previously Presented) The data processing system of
2 claim 34, wherein:
3 said first fixed size is an integral multiple of said second
4 fixed size; and
5 said exporter includes
6 a current packet register, and
7 a combiner connected to said current packet register and
8 said terminals, said combiner operable to
9 (a) store a current first information block in a
10 current packet register,
11 (b) sequentially select groups of the second fixed
12 size bits from the current packet register as a second
13 information block, a first selected group beginning at a
14 first bit of said current packet register, subsequent
15 selected groups beginning at a bit following a last bit
16 of a prior group, until all bits of the current packet
17 register are selected,

18 (c) thereafter store a next first information block
19 in the current packet register and repeat steps (a), (b)
20 and (c).

1 36. (Previously Presented) The data processing system of
2 claim 34, wherein:

3 said first fixed size is not an integral multiple of said
4 second fixed size; and

5 said exporter includes
6 a current packet register,
7 a last packet register, and
8 a combiner connected to said current packet register and
9 said terminals, said combiner operable to

10 (a) store a current first information block in a
11 current packet register,

12 (b) sequentially select groups of the second fixed
13 size bits from the current packet register as a second
14 information block, a first selected group beginning at a
15 next bit of said current packet register, subsequent
16 selected groups beginning at a bit following a last bit
17 of a prior group, until a number of bits of remaining in
18 the current packet register is less than the second fixed
19 number,

20 (c) store the current first information block in a
21 last packet register,

22 (d) store a next first information block in the
23 current packet register,

24 (e) select a group of the second fixed size bits
25 from a set of bits remaining in the last packet register
26 and bits starting at a first bit of the current packet
27 register, and

28 (f) thereafter repeat steps (b), (c), (d) and (e).

1 37. (Currently Amended) The method of Claim 2, including
2 performing said collecting at a data processor clock rate, and
3 performing said outputting at a transmission clock rate, wherein
4 the transmission clock rate is greater than the data processor
5 clock rate.

1 38. (Previously Presented) The method of Claim 1, wherein the
2 second fixed size is larger in size than the first fixed size.

1 39. (Currently Amended) The method of Claim 38, including
2 performing said collecting at a data processor clock rate, and
3 performing said outputting at a transmission clock rate, wherein
4 the transmission clock rate is less than the data processor clock
5 rate.

1 40. (Previously Presented) The method of claim 31, wherein:
2 said step of receiving the plurality of first information
3 blocks and arranging the emulation information contained therein
4 into a plurality of second information blocks wherein

5 said step (b) of sequentially selecting a group of the
6 second fixed size bits and said step (e) of selecting a group
7 of second fixed size bits stall if there is no first
8 information block stored in either said current packet
9 register or in said last packet register.

1 41. (Previously Presented) The method of claim 31, wherein:
2 said step of receiving the plurality of first information
3 blocks and arranging the emulation information contained therein
4 into a plurality of second information blocks wherein

5 said step (a) of storing a current first information
6 block in a current packet register and said step (d) of

7 storing a next first information block in the current packet
8 register stores NOP bits if no first information block is
9 available,

10 said step (b) of sequentially selecting a group of the
11 second fixed size bits and said step (e) of selecting a group
12 of second fixed size bits selects a group of a second fixed
13 size bits with a last valid first information block stored in
14 said current packet register or in said last packet register
15 and thereafter stalls if there is no first information block
16 stored in either said current packet register or in said last
17 packet register.

1 42. (Previously Presented) The method of claim 31, wherein:
2 said step of receiving the plurality of first information
3 blocks and arranging the emulation information contained therein
4 into a plurality of second information blocks wherein

5 said step (a) of storing a current first information
6 block in a current packet register and said step (d) of
7 storing a next first information block in the current packet
8 register stores NOP bits if no first information block is
9 available,

10 said step (b) of sequentially selecting a group of the
11 second fixed size bits and said step (e) of selecting a group
12 of second fixed size bits selects a group of a second fixed
13 size bits selects all NOP bits if there is no first
14 information block stored in either said current packet
15 register or in said last packet register.

1 43. (Currently Amended) The integrated circuit of Claim 17,
2 wherein said collector performs said collecting at a data
3 processor clock rate, wherein said exporter performs said
4 outputting at a transmission clock rate, and wherein the

5 transmission clock rate is greater than the data processor clock
6 rate.

1 44. (Previously Presented) The integrated circuit of Claim
2 16, wherein said second fixed size is greater in size than said
3 first fixed size.

1 45. (Currently Amended) The integrated circuit of Claim 44,
2 wherein said collector performs said collecting at a data
3 processor clock rate, wherein said exporter performs said
4 outputting at a transmission clock rate, and wherein the
5 transmission clock rate is less than the data processor clock
6 rate.

1 46. (Previously Presented) The integrated circuit of claim
2 33, wherein:
3 said combiner is further operable to
4 not sequentially select groups of the second fixed size
5 bits (b), not select a group of second fixed size bits (e) and
6 stall if there is no first information block stored in either
7 said current packet register or in said last packet register.

1 47. (Previously Presented) The integrated circuit of claim
2 33, wherein:
3 said combiner is further operable to
4 store NOP bits in a current packet register (a) and store
5 NOP bits in the current packet register if no first
6 information block is available,
7 sequentially select a group of the second fixed size bits
8 (b) and select a group of second fixed size bits (e) by
9 selecting a group of a second fixed size bits with a last
10 valid first information block stored in said current packet

11 register or in said last packet register and thereafter
12 stalling if there is no first information block stored in
13 either said current packet register or in said last packet
14 register.

1 48. (Previously Presented) The integrated circuit of claim
2 33, wherein:
3 said combiner is further operable to
4 store NOP bits in a current packet register (a) and store
5 NOP bits in the current packet register if no first
6 information block is available,
7 sequentially select a group of the second fixed size bits
8 (b) and select a group of second fixed size bits (e) by
9 selecting all NOP bits if there is no first information block
10 stored in either said current packet register or in said last
11 packet register.

1 49. (Currently Amended) The data processing system of Claim
2 34, wherein:
3 said collector performs said collecting at a data processor
4 clock rate;
5 said exporter performs said outputting at a transmission
6 clock rate; and
7 the transmission clock rate is greater than the data
8 processor clock rate.

1 50. (Previously Presented) The data processing system of
2 Claim 27, wherein:
3 said second fixed size is greater in size than said first
4 fixed size.

1 51. (Currently Amended) The data processing system of Claim

2 50, wherein:
3 said collector performs said collecting at a data processor
4 clock rate;
5 said exporter performs said outputting at a transmission
6 clock rate; and
7 the transmission clock rate is less than the data processor
8 clock rate.

1 52. (Previously Presented) The data processing system of
2 claim 36, wherein:
3 said combiner is further operable to
4 not sequentially select groups of the second fixed size
5 bits (b), not select a group of second fixed size bits (e) and
6 stall if there is no first information block stored in either
7 said current packet register or in said last packet register.

1 53. (Previously Presented) The data processing system of
2 claim 36, wherein:
3 said combiner is further operable to
4 store NOP bits in a current packet register (a) and store
5 NOP bits in the current packet register if no first
6 information block is available,
7 sequentially select a group of the second fixed size bits
8 (b) and select a group of second fixed size bits (e) by
9 selecting a group of a second fixed size bits with a last
10 valid first information block stored in said current packet
11 register or stored in said last packet register and thereafter
12 stalling if there is no first information block stored in
13 either said current packet register or in said last packet
14 register.

1 54. (Previously Presented) The data processing system of
2 claim 36, wherein:
3 said combiner is further operable to
4 store NOP bits in a current packet register (a) and store
5 NOP bits in the current packet register if no first
6 information block is available,
7 sequentially select a group of the second fixed size bits
8 (b) and select a group of second fixed size bits (e) by
9 selecting all NOP bits if there is no first information block
10 stored in either said current packet register or in said last
11 packet register.